

**REMARKS**

The Examiner rejected claims 21-42 under 35 U.S.C. §102(e) as being unpatentable over Mizuno et al. (U.S. Patent 6,711,071).

The Examiner rejected claims 21-42 under 35 U.S.C. §102(e) as being unpatentable over Bednar et al. (IEEE Managing Power and Performance for System-on-Chip Designs using Voltage Islands 2002).

Applicants respectfully traverse the §102(e) rejections with the following arguments.

35 USC § 102

As to Mizuno, et al.:

Applicants contend that claim 21, as amended, is not anticipated by Mizuno et al. because Mizuno et al. does not teach each and every feature of claim 21. As a first example Mizuno et al. does not teach "an externally supplied state saving power supply connected to a logic state saving circuit, ... said state saving circuit within either said voltage island  $V_1$  or said voltage island  $V_2$ ."

Applicants most strenuously point out that the concept of saving the state of logic circuits within voltages islands is unknown Mizuno et al.

Applicants believe the arguments presented *supra* with respect to claim 21 are also applicable to claim 31, as amended.

Based on the preceding arguments, Applicants respectfully maintain that claims 21 and 31 are not unpatentable over Mizuno et al. and are in condition for allowance. Since claims 22-30 and 41 depend from claim 21 and claims 32-40 and 42 depend from claim 31, Applicants respectfully maintain that claims 22-30, and 32-43 are likewise in condition for allowance.

As to claims 25 and 35, the Examiner indicated that elements VDDQ, VDD of FIG. 29 of Mizuno et al. are logic latches of a fencing means. Applicants point out that VDDQ is a power supply as is VDD and not latches. See for example, col. 4, lines 48-51.

As to claims 28 and 38, the Examiner has indicated that elements PWR1 and GEN1 of FIGs. 27-29 of Mizuno et al. are state saving latches. Applicants point out that element PWR1 is a power supply and not a state saving latch. See for example, FIGs. 27, 28 and 29 as well as col. 5, line 44. Applicants point out that element GEN1 is a voltage up converter and not a state saving latch. See for example, FIGs. 27, 28 and 29 and col. 5, lines 61-64.

As to claims 29 and 39, the Examiner has indicated that elements PWR1 and GEN1 of Mizuno et al. are power management state machines. Applicants point out that element PWR1 is a power supply and not a state saving latch. See for example, FIGs. 27, 28 and 29 as well as col. 5, line 44. Applicants point out that element GEN1 is a voltage up converter and not a state saving latch. See for example, FIGs. 27, 28 and 29 and col. 5, lines 61-64. Applicants most strenuously point out that the concept of state machines is unknown in Mizuno et al.

As to Bednar et al.:

Applicants point out Bednar et al. is a publication. Thus the rejections of claims 21-42 under 35 U.S.C. 102(e), to wit "(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent ..." is improper and must be withdrawn because the cited art is not a United States Patent.

Further applicants point out, Bednar et al. was presented at the 2002 IEEE/ACM international Conference on Computer-aided Design, 2002, San Jose, California, USA, November 10-14, 2002 by the inventors of the present patent application and that the IEEE lists its publication date as November 10-14, 2002.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

Respectfully submitted,  
FOR: Bednar et al.

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